JAPANESE PATENT OFFICE

PATENT JOURNAL

KOKAI PATENT APPLICATION NO. HEI 4[1992]-158565

Int. Cl.[5]: H 01 L 25/065
G 06 F 9/32
G 06 F 15/78
H 01 L 25/07
25/18
H 01 L 25/08

Sequence Nos. for Office Use: A 9198-5B
7638-4M
Z 7530-5L

Application No.: Hei 2[1990]-283762

Application Date: October 22, 1990

Publication Date: June 1, 1992

No. of Claims: 3 (Total of 11 pages)

Examination Request: Not requested

PROGRAM INSTRUCTION WORD-LENGTH-VARIABLE COMPUTER AND DATA PROCESSING DEVICE

Inventors: Takashi Tsukamoto
Epson-Seiko K.K.
3-3-5 Owa, Suwa-shi,
Nagano-ken

Sukuyuki Abe
Epson-Seiko K.K.
3-3-5 Owa, Suwa-shi,
Nagano-ken

Tetsuo Yabushita
c/o Epson-Seiko K.K.
3-3-5 Owa, Suwa-shi,
Nagano-ken

Yoshimitsu Hayashi
c/o Epson-Seiko K.K.
3-3-5 Owa, Suwa-shi,
Nagano-ken

Applicant: Epson-Seiko K.K.
2-4-1 Nishishinzuku,
Shinzuku-ku, Tokyo

Agent: Minoru Yamada, patent attorney

[There are no amendments to this patent.]

Claims

1. A program instruction word length-variable computer characterized by the use of a first semiconductor chip, which is constituted in accordance with the instruction word length housed in a program memory and includes an instruction register means, instruction decoder means, and timing generator means, along with a second semiconductor chip including a control part and an arithmetic logic part excluding each of the above-mentioned means; and in that it has a packing structure in which the first semiconductor chip is stacked in a down face state at the upper part of the second semiconductor chip and in which an electrical mutual connection of two chips is realized between the mutually opposite active surfaces of two chips.

2. A program instruction word-length-variable computer characterized by the use of a first package, in which a first semiconductor chip constituted in accordance with the instruction word length housed in a program memory and that includes an instruction register means, instruction decoder means, and timing generator means, is mounted, along with a second package, in which a second semiconductor chip including a control part and an arithmetic logic part excluding the above-mentioned each means, is mounted; and in that it has a packing structure in which the first package is stacked at the upper part of the second package and in which an electrical mutual connection of two chips is realized.

3. A data processing device characterized by the fact that the program instruction word-length-variable computer of Claim 1 or 2 is used.

* * *